Distributed Equivalent-Circuit Model for Traveling-Wave FET Design

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Abstract — **Based on reliable theoretical results, a distributed MESFET model is developed. It consists of equivalent-circuit elements which can be evaluated directly from FET material constants and geometry. The deviations with respect to full-wave-analysis results are investigated and some applications are shown.**

I. Introduction

THE DEVELOPMENT of so-called traveling-wave FET's (TWFET's) has given rise to numerous publications on this topic. In principle, there are two different concepts which must be distinguished: traveling-wave *amplifiers* using discrete FET cells connected by suitable transmission lines (e.g., [1]) and the nondiscrete TW*FET* configurations (e.g., [2]–[4]). The treatment presented in the following concentrates on the latter subject. When analyzing wave propagation, most of the authors adopt equivalent-circuit models [2], [3], whose elements, however, are not derived from realistic FET concepts and hence are questionable.

To establish results that are more reliable, the author developed a field-theoretical analysis in view of the need to model the FET by structures of growing complexity [5]–[7]. In this way, realistic information concerning wave propagation was obtained for the first time. It appeared, for instance, that low-loss approximations (as used in [2] and [3]) do not hold with regard to common FET's. Unfortunately, such a field-theoretical analysis needs a great amount of computing time and experience in connection with the root-searching process and is therefore not suitable for most practical applications.

On the other hand, these basic studies enable one now to create a novel distributed equivalent-circuit configuration which is based on this full-wave analysis and whose elements may be evaluated from any FET geometry. Using the field-theoretical results as a reference, the distributed-element configuration and its calculation from FET parameters can be optimized in such a way that only small deviations occur between a rigorous analysis and the equivalent-circuit formulation. This approach is the subject to be presented here. On the other hand, a detailed description of the wave propagation characteristics is beyond the scope of this paper. Such a description can be found in [7].

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II. The Model and Its Elements

In accordance with previous work [7], the FET is modeled by a structure of the type shown in Fig. 1. Longitudinal homogeneity is assumed. The waveguide properties of this configuration are then described by distributed equivalent-circuit elements, as can be seen from Fig. 2. Their evaluation will be explained in the following subsections. Note that they are distributed quantities.

For each element, as a first approach, the usual one-dimensional formula was applied assuming a simple homogeneous field distribution. The values obtained in this way were then checked against those calculated from the field-theoretical analysis [7]. If necessary, more elaborate physical formulas were adopted until fitting was satisfactory.

In contrast to common lumped-element concepts, our model includes the distributed properties. Therefore, the analysis concentrates on the longitudinal elements Z and L (see Fig. 2), whereas the channel is described by a first-order approach assuming a constant average depth (biasing at half the saturation current, one has approximately $h_3 = h_2/2$ (see Fig. 1)). The equivalent-circuit configuration consists of C_D, R_{gs}, and R_{gd} (see Fig. 2). A more detailed description, of course, may be implemented easily according to the usual lumped FET equivalent circuits.

Regarding Fig. 1, κ_S, κ_G, and κ_D refer to the metallic electrode conductivities ($\approx 3\cdot 10^7(\Omega\cdot\mathrm{m})^{-1}$). κ_{KS} denotes the conductivity of the low-field region of the channel ($\kappa_{KS} = en_D\mu_n$, with e being the electronic charge, n_D the donor concentration, and μ_n the mobility); R_{gd} represents the resistance of the high-field domain (see subsection II-D).

A. The Capacitances C_{s0}, C_{g0}, C_{d0}, C_D, C_{gs}, C_{gd}, and C_{ds}

It was found that the capacitances C_{s0}, C_{g0}, and C_{d0} and the depletion-layer capacitance C_D may be calculated by means of common simple formulas

$$C_{g0} = \epsilon_0\epsilon_S \frac{w_2 + d_1/2 + d_2/2}{h_1 - h_2}$$

$$C_{s0} = \epsilon_0\epsilon_S \frac{w_1 + d_1/2}{h_1 - h_2}. \quad (1)$$

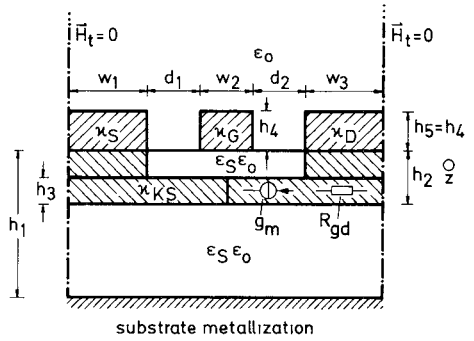


Fig. 1. Cross-sectional view of the FET structure under investigation. The parameters are, unless otherwise specified, as follows: $w_1 = w_3 = 4\ \mu m$; $w_2 = d_1 = d_2 = 1\ \mu m$; $h_1 = 30\ \mu m$; $h_2 = 0.2\ \mu m$; $h_3 = h_2/2 = 0.1\ \mu m$; $h_4 = h_5 = 1\ \mu m$; $\epsilon_S = 12.9$; $\kappa_G = \kappa_S = \kappa_D = 3 \cdot 10^7\ (\Omega \cdot m)^{-1}$; $\kappa_{KS} = 10\,000\ (\Omega \cdot m)^{-1}$; $R_{gd} = 0.12\ \Omega \cdot m$; and $g_m = 100$ mS/mm.

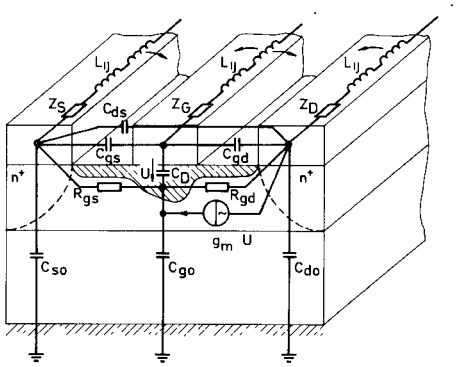


Fig. 2. The distributed equivalent circuit modeling the FET structure (the L_{ij} denote the elements of the outer inductance matrix (L)). All the elements represent distributed quantities.

The expression for C_{s0} gives the capacitance C_{d0} when replacing w_1 and d_1 by w_3 and d_2, respectively.

$$C_D = \epsilon_0 \epsilon_S \frac{w_2}{h_2 - h_3}. \tag{2}$$

More difficult is the evaluation of the interelectrode capacitances C_{gs}, C_{gd}, and C_{ds}. We proceed from the odd- and even-mode line capacitance of the equivalent coplanar waveguide (see Fig. 3). The odd-mode case (Fig. 3(a)) results in

$$C_{gs}^T = (\epsilon_S + 1)\epsilon_0 E\left(\frac{w_2}{w_2 + 2d_1}\right) + \epsilon_0 \frac{h_5}{d_1} + \epsilon_S \epsilon_0 \frac{h_2 - h_3}{2} \frac{1}{d_1} \tag{3}$$

with $E(X) = K(X)/K(\sqrt{1 - X^2})$ and $K(X)$ being the complete elliptic integral of the first kind. Correspondingly, C_{gd}^T can be obtained from (3) by replacing the variable d_1 with d_2. The first term in (3) represents the capacitance of the lower and upper half-planes for zero strip thickness and is well known from the literature [8], [9]. The second term takes into account the additional fields between the electrodes for nonzero strip thickness, and the third term includes the fringing capacitance between the gate electrode and the n^+ layer beneath the source and drain, respectively. It is, of course, of lower order of magnitude compared to the other two terms.

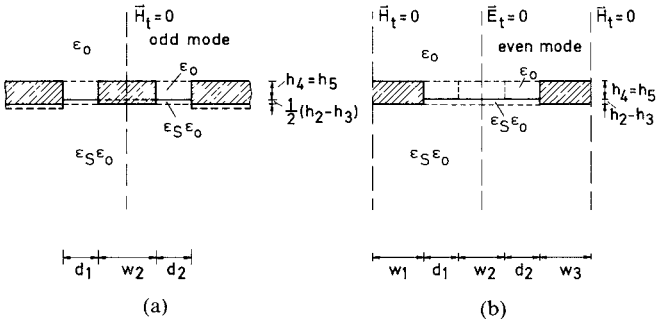


Fig. 3. The equivalent coplanar waveguide used to calculate C_{gs}^T, C_{gd}^T, and C_{ds}^T. (a) Odd-mode case. (b) Even-mode case (the CPW equivalence becomes obvious when removing the gate electrode and continuing the structure symmetric to the right-hand-side magnetic wall).

For the even-mode case (Fig. 3(b)), one derives, by similar considerations (including the magnetic walls),

$$C_{ds}^T = (\epsilon_S + 1)\epsilon_0 \frac{1}{2} E\left(\frac{1 + d/w}{(1 + d/2w)^2}\right) + \epsilon_0 \frac{h_5}{d_1 + d_2} + \epsilon_S \epsilon_0 \frac{h_2 - h_3}{d_1 + w_2 + d_2} \tag{4}$$

with $E(X)$ obtained from (3), $d = d_1 + w_2 + d_2$, and $w = \min\{w_1, w_3\}$.

The elements C_{gs}, C_{gd}, and C_{ds} have yet to be determined in such a way that the resulting odd- and even-mode capacitances of the circuit in Fig. 2 equate C_{gs}^T, C_{gd}^T, and C_{ds}^T, respectively. One finds

$$C_{gs} = C_{gs}^T - \frac{C_{xg}C_{s0}}{C_{xg} + C_{s0} + C_{d0}} \quad C_{gd} = C_{gd}^T - \frac{C_{xg}C_{d0}}{C_{xg} + C_{s0} + C_{d0}} \tag{5}$$

with C_{gs}^T and C_{gd}^T obtained from (3) and

$$C_{xg} = \frac{C_{g0}C_D}{C_{g0} + C_D}$$

and

$$C_{ds} = C_{ds}^T - \left\{\frac{1}{C_1} + \frac{1}{C_2 C_{gd}/(C_2 + C_{gd}) + C_3 C_{d0}/(C_3 + C_{d0})}\right\}^{-1}$$

$$C_1 = C_{s0} + C_{gs} + \frac{C_{gs}C_{s0}}{C_{xg}} \quad C_2 = C_{xg} + C_{gs} + \frac{C_{gs}C_{xg}}{C_{s0}},$$

$$C_3 = C_{xg} + C_{s0} + \frac{C_{s0}C_{xg}}{C_{gs}}. \tag{6}$$

C_{ds}^T is obtained from (4), and C_{xg} from (5).

Regarding the case of symmetry ($w_1 = w_3$, $d_1 = d_2$), eqs. (5) and (6) reduce to relatively simple expressions.

B. The Outer Inductances L_{ij}

For convenience, the outer mutual and self-inductances are written in matrix notation. It is commonly assumed that these inductances vary only slightly when dielectrics

or losses are introduced to the waveguide geometry. Then (L) may be calculated from the capacitance matrix of the corresponding loss-free structure with homogeneous $\epsilon_r = 1$ (e.g. [4] and [9]). It was found from the field-theoretic analysis that this basic assumption holds quite well regarding the problem under consideration.

Consequently, one obtains

$$(L) = \mu_0 \epsilon_0 \cdot (C_0)^{-1} \tag{7}$$

with (C_0) being the matrix of the capacitances in Fig. 2 for the case where $\epsilon_S = 1$ and $g_m = R_{gs} = R_{gd} = 0$.

C. The Longitudinal Impedances of the Electrodes (Z_S, Z_G, Z_D)

Z_S, Z_G, and Z_D are complex quantities. The real part represents the electrode resistance, the imaginary part the inner inductance. In the frequency range of interest and for realistic electrode dimensions, neither the dc current nor the skin-effect approximation holds with sufficient accuracy. Hence, according to [10], a closed-form expression is used to calculate the source and drain electrode impedances Z_S and Z_D ((8) yields Z_D if w_1 and κ_S are replaced by w_3 and κ_D, respectively):

$$Z_S = \frac{1}{w_1} \frac{\gamma_S}{\kappa_S} \coth(\gamma_S h_5) \tag{8}$$

with

$$\gamma_S = (1+j)\sqrt{\frac{\omega \mu_0 \kappa_S}{2}}.$$

Because of its position in the center between the source and drain, the gate electrode cross section is separated into two equal parts for evaluating Z_G, each of them with half the thickness. The impedances of these two half-sections can be derived as done before (see (8)). They are connected in parallel and in this way we have

$$Z_G = \frac{1}{2} \cdot \frac{1}{w_G} \frac{\gamma_G}{\kappa_G} \coth\left(\gamma_G \cdot \frac{h_G}{2}\right)$$

with

$$\gamma_G = (1+j)\sqrt{\frac{\omega \mu_0 \kappa_G}{2}} \tag{9}$$

$w_G = \max\{w_2, h_4\}$ and $h_G = \min\{w_2, h_4\}$.

D. The Channel Resistances R_{gs} and R_{gd}

R_{gs} corresponds to the low-field region of the channel and can be approximated by

$$R_{gs} = \frac{1}{\kappa_{KS}} \frac{d_1 + w_2/2}{h_3}. \tag{10}$$

On the other hand, R_{gd} describes the high-field domain beneath the drain end of the gate. Common equivalent circuits indicate a resistance of about 400 Ω for each 300 μm of gate width, nearly independent of geometry. This corresponds to a constant R_{gd} of 0.12 Ω·m.

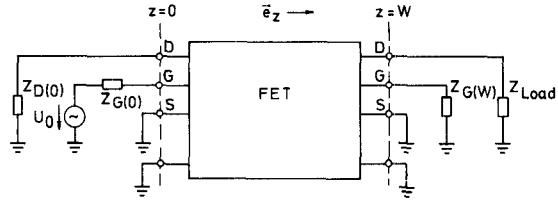


Fig. 4. The FET and one possible setup configuration. The FET is modeled by distributed equivalent circuits according to Fig. 2.

III. Wave Propagation Analysis

For convenience, matrix notation is used to study wave propagation along the electrodes (z axis). The elements in the plane perpendicular to the z axis form the admittance matrix (Y). (Z) denotes the diagonal matrix containing the electrode impedances Z_S, Z_G, and Z_D, and (L) the outer inductance matrix (see subsection II-B). One derives

$$\frac{\partial}{\partial z}(U) = -\{(Z) + j\omega(L)\} \cdot (I) \Big| \frac{\partial}{\partial z}(I) = -(Y) \cdot (U) \tag{11}$$

and, assuming voltages and currents $\sim \exp\{j(\omega t - k_z z)\}$,

$$\{[(Z) + j\omega(L)] \cdot (Y) + k_z^2 \cdot (E)\} \cdot (U) = 0 \tag{12}$$

with (E) the matrix of unity. Substituting $k_z = \pm\sqrt{-\lambda}$, eq. (12) represents a standard eigenvalue problem $\{(A) - \lambda(E)\} \cdot (X) = 0$. The eigenvalues λ_i give the complex propagation constants of the three fundamental modes, and the corresponding eigenvectors deliver the current and voltage distribution of each mode. Superposition of the forward- and backward-traveling waves of the three modes with unknown amplitudes constitutes the resulting total currents and voltages on source, gate, and drain, respectively.

Applying a fixed gate width W and introducing the termination conditions at each port of the transistor, one is able to derive the impedance matrix and, therefrom, all quantities of interest (e.g., scattering coefficients) [7]. Fig. 4 shows one possible configuration of the termination network.

A Fortran computer program was written that calculates the elements in Fig. 2, solves wave propagation as explained above, and evaluates the different quantities as desired. For example, computing the plot of Fig. 6(a) with 200 points per curve consumes about 70 seconds CPU time on the IBM 370/168 at the Technische Hochschule Darmstadt. Compared with the corresponding field-theoretic calculation of [7], CPU time is reduced by a factor of more than 100!

IV. Comparison with Field-Theoretic Results

Regarding FET design, the deviations of propagation constants and characteristic impedances are less important than those of the resulting input–output characteristics, such as input impedance or feedback terms. Hence, an error quantity E_{max} is considered that stands for the

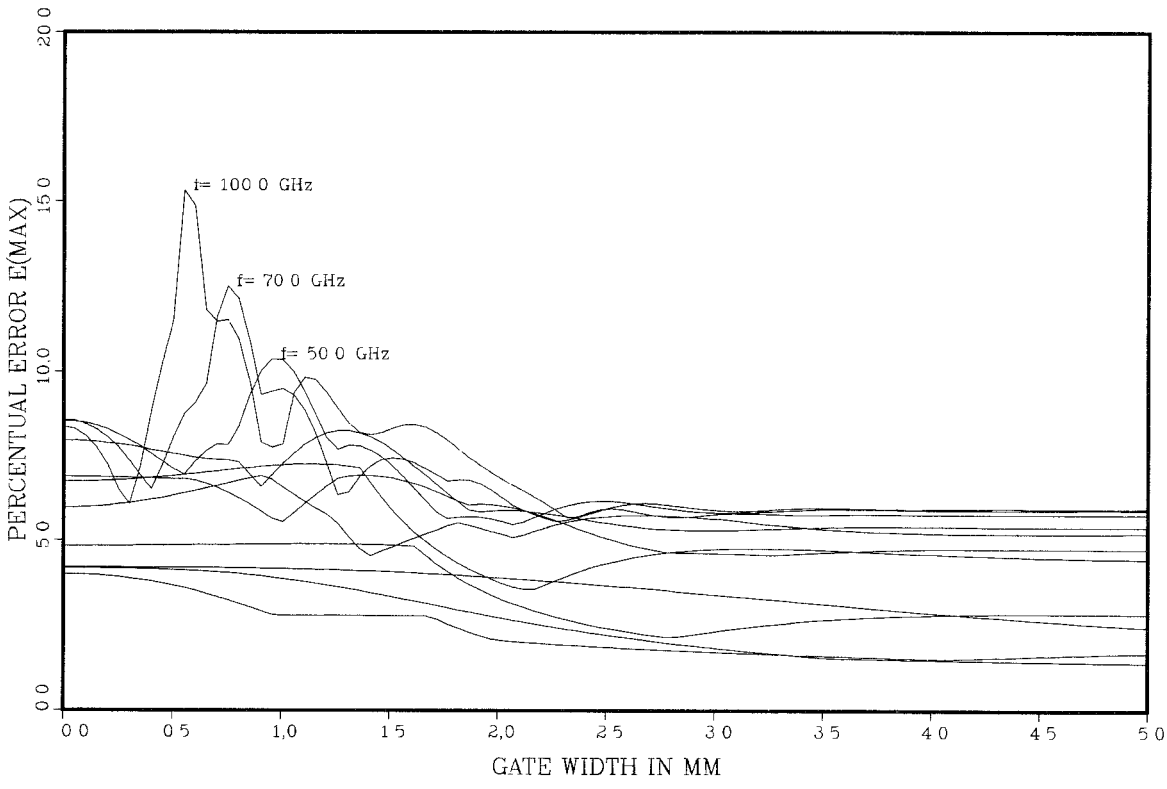
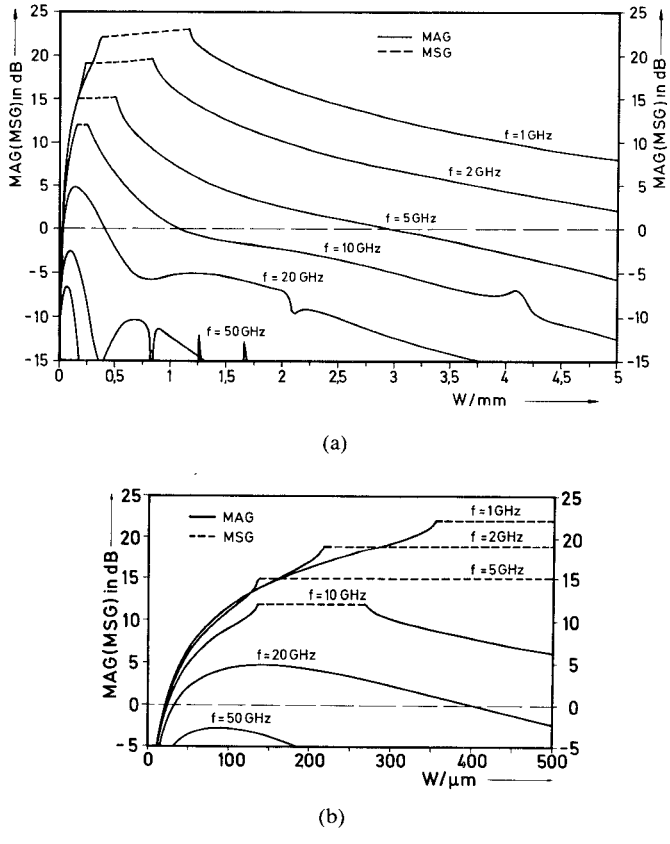


Fig. 5. Equivalent circuit model (Fig. 2) compared with full-wave analysis [7]. The maximum deviations of Z and Y matrix elements against gate width W for different frequencies f ($f = 0.1$–100 GHz).



(a)

(b)

Fig. 6. Maximum available gain (MAG) and maximum stable gain (MSG) as a function of gate width W. Frequency is the curve parameter. (1-μm FET data from Fig. 1; common gate-in drain-out configuration is considered with $Z_{G(W)} = Z_{D(0)} = 1$ kΩ (see Fig. 4).)

deviations of the resulting FET impedance and admittance matrices when compared to full-wave analysis [7]. As can be seen from Fig. 5, this error $E_{\max}$ ranges around 10 percent.

For experimental verification, special four-port MESFET structures were fabricated. The measured data show encouraging agreement; a more detailed description, however, would exceed the limits of this paper.

V. Some Results

An example shall be treated here demonstrating the feasibilities of the model presented in Section II.

In [7], the channel is considered to possess a spatial-constant conductivity value. This assumption was made to reduce excessive numerical efforts due to the elaborated full-wave analysis. Regarding real FET's, however, such an approach will cause certain errors. Improved results are now given in Fig. 6, letting $R_{gs} \neq R_{gd}$ in our model. One finds that the principal behavior of the curves has not changed compared with [7]. The channel-conductivity nonsymmetry, however, results in an increased MAG (or MSG, respectively) at frequencies below 20 GHz and in a MAG degradation at higher frequencies.

Fig. 6(b) shows details when discussing the optimal gate width W_{opt} at which the gain maximum occurs. Due to the high losses, W_{opt} remains small compared to the wavelength. The model of Fig. 2 was also employed successfully for further investigations concerning the limits of lumped-element FET modeling [11].

VI. Conclusions

The distributed equivalent-circuit model approximates the results from our full-wave analysis [7] with good accuracy. Compared to the latter treatment, the efforts in CPU time and computer storage are reduced drastically. In contrast to other developments to date [2], [3], the elements of the equivalent circuit can be calculated directly from FET parameters, such as geometry and material properties. That offers interesting features concerning CAD applications and FET design.

Since the circuit elements are not derived by means of curve fitting but by physical considerations, the model obtained is expected to produce reliable results also for parameter constellations (see Section V) that cannot be checked against full-wave references.

Finally, one should stress that the possible applications of such a wave propagation treatment are *not* restricted to TWFET design. Based on the concepts presented here, advanced models for standard microwave FET's can be developed, too, which take into account their distributed properties.

Acknowledgment

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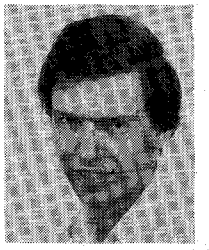

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